REMARKS

Preliminary Matter

Applicant thanks the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119 and receipt of the certified copy of the priority document. Applicant also thanks the Examiner for considering the references cited with the Information Disclosure Statement filed November 20, 2003. The Examiner's approval of the drawings is further appreciated.

Status of the Application

Claims 1-8 have been examined and are all the claims pending in the application. Applicant herein amends claims 1-8 for reasons of precision of language. Applicant submits that the amendments to the claims were made merely to more accurately claim the present invention and do not narrow the literal scope of the claims and thus do not implicate estoppel in the application of the doctrine of equivalents.

Claim Rejections - 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-8 under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 7,000,140 to Okubo (hereinafter "Okubo") in view of U.S. Patent No. 4,434,696 to Conviser (hereinafter "Conviser"). Applicants submit that the claims are patentable.

For example, claim 1 recites a clock control means for changing a frequency multiplication ratio of a frequency multiplication circuit to 1/N and changing a frequency division ratio of a second frequency division circuit to 1/N.

Okubo is directed to a data processor which includes a CPU 2 which can execute an instruction, a clock pulse generator 3 that enables frequency multiplication and frequency division operation to a clock signal and outputs synchronizing clock signals CLK1, CLK2. The clock pulse generator 3 includes a PLL circuit 41 for multiplying a source clock signal 13, and frequency dividers 43, 44 which frequency divide the output of the PLL circuit 41 and output clock signals CLK1, CLK2 via selectors 45, 46 and output circuits 47, 48. Clock signal CLK1 is supplied to a built-in peripheral circuit 7, and clock signal CLK2 is supplied to the CPU 2. The supply of the clock signals CLK1, CLK2 are suppressed or enabled based on a mode of operation of the data processor.

The Examiner contends that Okubo's PLL circuit 41 corresponds to the claimed frequency multiplication circuit and that Okubo's frequency divider 44 corresponds to the claimed second frequency division circuit. However, referring to column 2, lines 11-28 of Okubo, the frequency multiplication and frequency division operation in the clock pulse generator 3 are *enabled* or *suspended*, and the clock signals CLK1, CLK2 are *supplied* or *stopped* depending on the mode of operation. Thus, Okubo does not teach or suggest *changing* a frequency multiplication ratio of the alleged frequency multiplication circuit 41 to 1/N and *changing* a frequency division ratio of the alleged second frequency division circuit 44 to 1/N as required by claim 1. On page 3 of the Office Action, the Examiner admits that Okubo does not teach or suggest the capability of showing the multiplication ratio of the PLL circuit 44 as 1/N and cites Conviser to supply this deficiency.

Conviser is directed to an instrument for comparing equal temperament and just intonation including a master-oscillator which supplies a primary reference frequency to a modulo-N counter. The modulo-N counter is used as a frequency divider whose divided frequency serves as the input signal to a phase-locked loop (PLL) having an output frequency controlled by a second Modulo-M counter, which operates as a multiplier. Thus, a ratio of M/N is established for the two outputs.

The Examiner asserts that the ratio provided by Conviser's Modulo-M counter corresponds to the claimed 1/N frequency ratio. However, the Examiner does not indicate how the Conviser's instrument would be combined with Okubo's data processor. If the Examiner alleges that Conviser's frequency divider having a ratio of N which contributes a ratio of 1/N corresponds to Okubo's frequency divider 44 and the claimed second frequency division circuit, then it seems the Examiner would assert that Conviser's frequency multiplier corresponds to Okubo's PLL circuit 41 and the claimed frequency multiplication circuit. However, Conviser's alleged frequency multiplication circuit (frequency multiplier) has a ratio of M which contributes to the M/N ratio. Thus, Conviser does not teach or suggest changing a frequency multiplication ratio of a frequency multiplication circuit to 1/N and changing a frequency division ratio of a second frequency division circuit to 1/N as required by claim 1.

Because Okubo and Conviser, neither alone nor in combination, teach all of the features of claim 1, Applicant submits that claim 1 is patentable and respectfully requests withdrawal of the rejection. Because independent claims 3, 5, and 7 recite features analogous to those recited in claim 1, Applicant submits that these claims are patentable at least for reasons analogous to

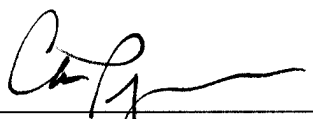
those discussed above regarding claim 1. Applicant also submits that claims 2, 4, 6, and 8, being dependent on claims 1, 3, 5, and 7, respectively, are patentable at least by virtue of their dependency. Thus, withdrawal of the rejection is respectfully requested.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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